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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,247	11/21/2001	Binneg Y. Lao	89252.0005	2160

26021 7590 11/05/2003

HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
PERKINS, PAMELA E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 11/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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7590 03/14/2003

Soyeon (Karen) P. Laub
Sierra Monolithics, Inc.
Suite 102
103 W. Torrance Blvd.
Redondo Beach, CA 90277

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Office Action Summary	Application No.	Applicant(s)	
	09/990,247	LAO ET AL.	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,12-28,31-33,35-44,46,48-53 and 55-59* is/are rejected.

7)☒ Claim(s) *3,9-11,29,30,34,45,47 and 54* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the filing of the application papers on 21 November 2001.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6, 8, 12, 15, 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugino et al. (5,373,187) in view of Walz (5,307,237).

Sugino et al. disclose a method for connecting at least one high speed integrated circuit (IC) chip to external terminals, where the IC has a plurality of signal pad the method comprising a substrate (10), forming a plurality of microstrips on the substrate (10), wherein the microstrips provide transmission between a plurality of signal pads and external terminals and have a substantially constant characteristic impedance throughout substantially the entire length (col. 12, line 54 thru col. 13, line 10). Sugino et al. further disclose microstrips with a first end to receiving signals, some of the microstrips connecting to high speed signals, wherein the high speed signal does not transmit through the substrate and some of the microstrips connecting to low speed signals (col. 14, line 58 thru col. 15, line13). Sugino et al. also disclose the substrate

comprises multiple layers (col. 14, lines 47-57). Sugino et al. do not disclose at least a pair of the microstrips are capacitively coupled to each other.

Walz discloses disclose a method for connecting at least one high speed IC chip to external terminals, where the IC has a plurality of signal pad the method comprising a substrate, forming a plurality of microstrips on the substrate, wherein the microstrips provide transmission between a plurality of signal pads and external terminals. Walz further discloses at least a pair of the microstrips are capacitively coupled to each other and have substantially constant characteristic impedance throughout substantially the entire length of the pair (equivalent abstract).

Since Sugino et al. and Walz are both from the same field of endeavor, a method for connecting at least one high-speed IC chip to external terminals, the purpose disclosed by Walz would have been recognized in the pertinent art of Sugino et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Sugino et al. by a pair of the microstrips are capacitively coupled to each other as taught by Walz to reduce signal degradation (advantage).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugino et al. in view of Walz as applied to claims 1, 8, 15, 16 and 20 above, and further in view of Hill (6,028,348).

Sugino et al. disclose a method for connecting at least one high speed integrated circuit (IC) chip to external terminals, where the IC has a plurality of signal pad the method comprising a substrate (10), forming a plurality of microstrips on the substrate

(10), wherein the microstrips provide transmission between a plurality of signal pads and external terminals and have a substantially constant characteristic impedance throughout substantially the entire length (col. 12, line 54 thru col. 13, line 10). Sugino et al. further disclose microstrips with a first end to receiving signals, some of the microstrips connecting to high speed signals, wherein the high speed signal does not transmit through the substrate and some of the microstrips connecting to low speed signals (col. 14, line 58 thru col. 15, line13). Sugino et al. also disclose the substrate comprises multiple layers (col. 14, lines 47-57). Sugino et al. do not disclose the substrate is made of alumina.

Hill discloses a method for connecting at least one high speed IC chip to external terminals where a plurality of microstrips are formed on a substrate, wherein the microstrips provide transmission between a plurality of signal pads and external terminals. Hill further disclose the substrate as made of alumina (col. 3, lines 52-63).

Since Sugino et al. and Hill are both from the same field of endeavor, a method for connecting at least one high speed IC chip to external terminals, the purpose disclosed by Hill would have been recognized in the pertinent art of Sugino et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Sugino et al. by the having substrate is made of alumina as taught by Hill to reduce thermal resistance (col. 1,lines 29-40).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugino et al. in view of Walz as applied to claims 1, 8, 15, 16 and 20 above, and further in view of Asous (5,995,261).

Sugino et al. disclose a method for connecting at least one high speed integrated circuit (IC) chip to external terminals, where the IC has a plurality of signal pad the method comprising a substrate (10), forming a plurality of microstrips on the substrate (10), wherein the microstrips provide transmission between a plurality of signal pads and external terminals and have a substantially constant characteristic impedance throughout substantially the entire length (col. 12, line 54 thru col. 13, line 10). Sugino et al. further disclose microstrips with a first end to receiving signals, some of the microstrips connecting to high speed signals, wherein the high speed signal does not transmit through the substrate and some of the microstrips connecting to low speed signals (col. 14, line 58 thru col. 15, line13). Sugino et al. also disclose the substrate comprises multiple layers (col. 14, lines 47-57). Sugino et al. do not disclose the microstrips have a 50-ohm transmission line throughout substantially the entire length of the microstrips.

Asous discloses a method for connecting at least one high-speed IC chip to external terminals where a plurality of are formed microstrips on a substrate. Asous further disclose the microstrips is 50-ohm transmission line throughout substantially the entire length of the microstrips (col. 3, lines 11-24).

Since Sugino et al. and Asous are both from the same field of endeavor, a method for connecting at least one high-speed IC chip to external terminals, the

purpose disclosed by Asous would have been recognized in the pertinent art of Sugino et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Sugino et al. by the microstrips have a 50-ohm transmission line throughout substantially the entire length of the microstrips as taught by Asous to carry high frequencies without distortion (col. 3, lines 23 and 24).

Claims 14, 21-25, 27, 28, 33, 35, 36, 38, 41-43, 46, 48, 50-53, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugino et al. in view of Walz as applied to claims 1, 8, 15, 16 and 20 above, and further in view of Aruga (6,486,755).

Sugino et al. disclose a method for connecting at least one high speed integrated circuit (IC) chip to external terminals, where the IC has a plurality of signal pad the method comprising a substrate (10), forming a plurality of microstrips on the substrate (10), wherein the microstrips provide transmission between a plurality of signal pads and external terminals and have a substantially constant characteristic impedance throughout substantially the entire length (col. 12, line 54 thru col. 13, line 10). Sugino et al. further disclose microstrips with a first end to receiving signals, some of the microstrips connecting to high speed signals, wherein the high speed signal does not transmit through the substrate and some of the microstrips connecting to low speed signals (col. 14, line 58 thru col. 15, line13). Sugino et al. also disclose the substrate comprises multiple layers (col. 14, lines 47-57). Sugino et al. do not disclose the signal are differential signals, the high-speed signal does not transmit through the substrate,

forming interconnects within the substrate which provide connection between the substrate through a via and the terminals as ball grid array (BGA) terminals.

Aruga discloses a method for connecting at least one high speed IC chip to external terminals where a plurality of are formed microstrips on a substrate, the substrate comprising multiple dielectric layers (col. 2, lines 43-56), wherein the microstrips provide transmission between a plurality of signal pads and external terminals; wherein the signal does not transmit through the substrate (col. 9, lines 31-44). Aruga further discloses the signal are differential signals (6, lines 4-7), forming interconnects within the substrate which provide connection between the substrate through a via (col. 6, lines 24-29) and the terminals as ball grid array (BGA) terminals (col. 8, lines 36-43).

Since Sugino et al. and Aruga are both from the same field of endeavor, a method for connecting at least one high-speed IC chip to external terminals, the purpose disclosed by Aruga would have been recognized in the pertinent art of Sugino et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Sugino et al. by having the signal are differential signals, not transmitting the signal through the substrate, forming interconnects within the substrate which provide connection between the substrate through a via and the terminals as ball grid array (BGA) terminals as taught by Aruga to minimize the influences of exterior noises (col. 1,lines 24-30).

Claims 2, 31, 37, 39, 40, 44 and 57-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugino et al. in view of Walz and Aruga as applied to claims 1, 8, 14-16, 20, 21-25, 27, 28, 33, 35, 36, 38, 41-43, 46, 48, 50-53, 55 and 56 above, and further in view of Garland et al. (6,441,697).

Sugino et al. disclose a method for connecting at least one high speed integrated circuit (IC) chip to external terminals, where the IC has a plurality of signal pad the method comprising a substrate (10), forming a plurality of microstrips on the substrate (10), wherein the microstrips provide transmission between a plurality of signal pads and external terminals and have a substantially constant characteristic impedance throughout substantially the entire length (col. 12, line 54 thru col. 13, line 10). Sugino et al. further disclose microstrips with a first end to receiving signals, some of the microstrips connecting to high speed signals, wherein the high speed signal does not transmit through the substrate and some of the microstrips connecting to low speed signals (col. 14, line 58 thru col. 15, line13). Sugino et al. also disclose the substrate comprises multiple layers (col. 14, lines 47-57). Sugino et al. do not disclose the width of the microstrips increasing as it is outwardly routed and the substrate is ceramic.

Garland et al. disclose a method for connecting at least one high speed IC chip to external terminals where a plurality of microstrips are formed on a substrate, wherein the width of the microstrips increasing as it is outwardly routed (col. 5, lines 57-67). Garland et al. further disclose the substrate is ceramic (col. 7, lines 19-36).

Since Sugino et al. and Garland et al. are both from the same field of endeavor, a method for connecting at least one high-speed IC chip to external terminals, the

purpose disclosed by Garland et al. would have been recognized in the pertinent art of Sugino et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Sugino et al. by the width of the microstrips increasing as it is outwardly routed and the substrate is ceramic as taught by Garland et al. to carry high frequencies without distortion (col. 1, lines 6-11).

Claims 5, 7, 17-19, 26, 32 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugino et al. in view of Walz and Aruga as applied to claims 1, 8, 14-16, 20, 21-25, 27, 28, 33, 35, 36, 38, 41-43, 46, 48, 50-53, 55 and 56 above, and further in view of *applicant's prior art*.

Sugino et al. disclose a method for connecting at least one high speed integrated circuit (IC) chip to external terminals, where the IC has a plurality of signal pad the method comprising a substrate (10), forming a plurality of microstrips on the substrate (10), wherein the microstrips provide transmission between a plurality of signal pads and external terminals and have a substantially constant characteristic impedance throughout substantially the entire length (col. 12, line 54 thru col. 13, line 10). Sugino et al. further disclose microstrips with a first end to receiving signals, some of the microstrips connecting to high speed signals, wherein the high speed signal does not transmit through the substrate and some of the microstrips connecting to low speed signals (col. 14, line 58 thru col. 15, line13). Sugino et al. also disclose the substrate comprises multiple layers (col. 14, lines 47-57). Sugino et al. do not disclose a

dielectric ring portion of the coaxial terminals with a width substantially equal to the thickness of the substrate and the external terminals as coaxial GPPO connectors.

Applicant's prior art discloses a method for connecting at least one high speed IC chip to external terminals where a plurality of microstrips are formed on a substrate, wherein the microstrips provide transmission between a plurality of signal pads and external terminals (page 2). *Applicant's prior art* further discloses a dielectric ring portion of the coaxial terminals with a width substantially equal to the thickness of the substrate and the external terminals as coaxial GPPO connectors (page 3).

Since Sugino et al. and *applicant's prior art* are both from the same field of endeavor, a method for connecting at least one high speed IC chip to external terminals, the purpose disclosed by *applicant's prior art* would have been recognized in the pertinent art of Sugino et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Sugino et al. by a dielectric ring portion of the coaxial terminals with a width substantially equal to the thickness of the substrate and the external terminals as coaxial GPPO connectors as taught by the *applicant's prior art* to increase the signal and frequencies of IC chips (page 2).

Referring to claims 6, 12, 22, 43, 51 and 56, Sugino et al. or do not disclose an operating frequency of 20 Gbps or greater, a microstrip partial length no more than 5 mils and a substrate less than o.4 cubic inches. It would have been obvious to one having ordinary skill in the art at the time invention was made to an operating frequency of 20 Gbps, a microstrip partial length no more than 5 mils and a substrate less than o.4

cubic inches disclosed in the claimed invention, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Allowable Subject Matter

Claims 3, 9-11, 29, 30, 34, 47 and 54 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: prior art does not anticipate, teach, or suggest a method of connecting an IC chip where the width of microstrip is increase with the capacitance to maintain contact impedance and forming layers using a high-temperature or low-temperature co-fired ceramics process.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (703) 605-4299. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

pep
March 10, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800